

FORM PT01449
(REV. 8-83)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.
HARI.006UST

SERIAL NO.
09/143,233

INFORMATION DISCLOSURE STATEMENT
(Use several sheets if necessary)

APPLICANT
Eliyahou Harari et al.

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August 28, 1998

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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LVH	A6 4 0 5 1 3 5 4	09/1977	Choate			
LVH	A7 4 0 6 6 8 8 0	01/1978	Salley			
LVH	A8 4 0 8 7 7 9 5	05/1978	Rossler			
LVH	A9 4 1 8 1 9 8 0	01/1980	McCoy			
LVH	A10 4 2 7 9 0 2 4	07/1981	Schrenk			
LVH	A11 4 2 8 7 5 7 0	09/1981	Stark			
LVH	A12 4 3 5 7 6 8 5	11/1982	Daniele et al.			
LVH	A13 4 3 6 5 3 1 8	12/1982	Aichelmann Jr. et al.			
LVH	A14 4 4 2 2 1 6 1	12/1983	Kressel et al.			
LVH	A15 4 4 3 0 7 2 7	02/1984	Moore et al.			
LVH	A16 4 4 4 8 4 0 0	05/1984	Harari			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS. (YES/N)
B1 JP 58 2 1 5 7 9 4	1983	Japan			Abstrac
B2 JP 60 0 7 6 0 9 7	04/1985	Japan			Abstrac
B3 JP 59 0 4 5 6 9 5	1984	Japan			Abstrac
B4 JP 59 1 6 2 6 9 5	1984	Japan			Abstrac
B5 JP 63 1 8 3 7 0 0	07/1988	Japan			Abstrac

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

LVH	C1	Torelli, Guido "An LSI Technology Fully Compatible EAROM Cell", S-ATES Componenti Elettronici SpA, no. 6, vol. LI, 7 pp., 1982.
LVH	C2	Berenga et al. "E2-PROM TV Synthesizer", 1978 IEEE International Solid-State Circuits Conference: ISCCC 78," February 17, 1978, pp.196-197.
LVH	C3	Lucerno et al. "A 16 kbit Smart 5 V-only EEPROM with Redundancy", IEEE Journal of Solid-State Circuits, Vol. SC-18, no. 5, pps. 539-543, October 1983.

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U. S. PATENT DOCUMENTS				MAILED August 28, 1998		GROUP 2785 Group 2700	
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE	
RV 2/3/11 LWH	A17	4 4 6 0 9 8 2	07/1984	Gee et al.			
LWH	A18	4 4 9 3 0 7 5	01/1985	Anderson et al.			
LWH	A19	4 5 2 5 8 3 9	06/1985	Nozawa et al.			
LWH	A20	4 5 2 7 2 5 1	07/1985	Nibby Jr. et al.			
LWH	A21	4 5 2 8 6 8 3	07/1985	Henry			
LWH	A22	4 5 6 2 5 3 2	12/1985	Nishizawa et al.			
LWH	A23	4 6 0 8 6 7 1	08/1986	Shimizu et al.			
LWH	A24	4 6 1 2 6 4 0	09/1986	Mehrotra et al.			
LWH	A25	4 6 1 6 3 1 1	10/1986	Sato			
LWH	A26	4 6 1 7 6 5 1	10/1986	Ip et al.			
LWH	A27	4 6 3 8 4 5 7	01/1987	Schrenk			
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LWH	B6	JP 58 2 1 5 7 9 5	12/1983	Japan		Abstrac	
LWH	B7	JP 63 2 0 0 3 9 8	08/1988	Japan		Abstrac	
LWH	B8	JP 62 2 8 3 4 9 6	12/1987	Japan		Abstrac	
LWH	B9	JP 54 1 5 8 1 4 1	12/1979	Japan		Abstrac	
LWH	B10	JP 58 0 6 0 4 9 3	04/1983	Japan		Abstrac	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)							
LWH	C4	Stark Moshe, "Two Bits Per Cell ROM", Digest of Papers of Spring COMPCONS 81, Feb. 23-26, VLSI LABORATORY, pp. 209-212.					
LWH	C5	Torelli et al, "An Improved Method for Programming a Word-Erasable EEPROM", Alta Frequenza, Vol. 52, Nov. - Dec. 1983, no. 6, pp. 487-494.					
LWH	C6	Harold, "Production EPROM Loading", New Electronics, Vol. 15 (1982) Feb. 1982, No. 3, London, Great Britain, pp. 46-50.					
EXAMINER Ly V. Hua				DATE CONSIDERED 12/14/99			
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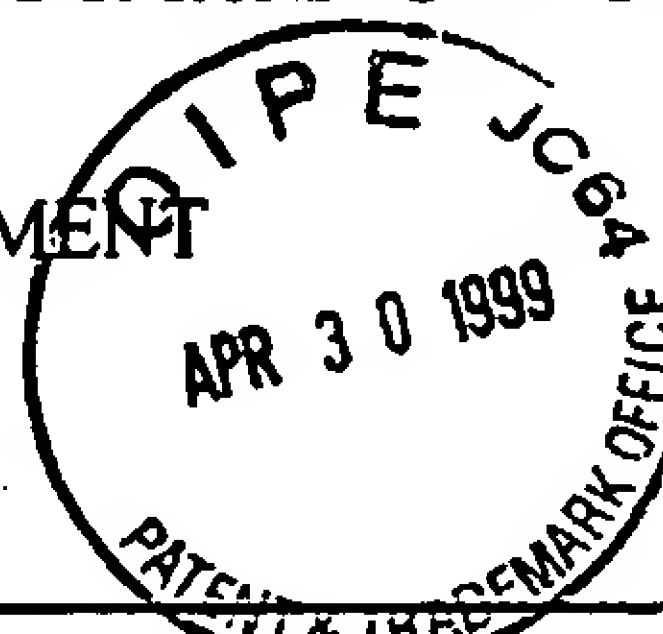
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*EXAMINER INITIAL		DOCUMENT NUMBER								DATE	NAME	CLASS	SUB CLASS	FILING DATE
RL	A28	4	6	5	2	8	9	7		03/1987	Okuyama et al.			
RL	A29	4	6	6	3	7	7	0		05/1987	Murray et al.			
RL	A30	4	6	6	7	2	1	7		05/1987	Janning			
RL	A31	4	6	8	2	2	8	7		07/1987	Mizuno et al.			
RL	A32	4	7	1	8	0	4	1		01/1988	Baglee et al.			
RL	A33	4	7	3	3	3	9	4		03/1988	Giebel			
RL	A34	4	7	5	7	4	7	4		07/1988	Fukushi et al.			
RL	A35	4	7	6	3	3	0	5		08/1988	Kuo			
RL	A36	4	7	7	4	7	0	0		09/1988	Satoh et al.			
RL	A37	4	8	0	0	5	2	0		01/1989	Iijima			
RL	A38	4	8	0	3	7	0	7		02/1989	Cordan Jr.			

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		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS. (YES/N)
RL	B11	JP	58	0	8	6	7	7	7	05/1983	Japan			Abstrac
RL	B12	JP	62	2	8	3	4	9	7	12/1987	Japan			Abstrac
RL	B13	FR	2	4	3	0	0	6	5	01/1980	France			Abstrac
RL	B14	DE	3	2	0	0	8	7	2	07/1983	Germany			Abstrac
RL	B15	EP	0	2	5	1	8	8	9	01/1988	EPO			Abstrac

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

RL	C7	Alberts et al., "Multi-Bit Storage Fet Earom Cell", IBM Technical Disclosure Bulletin," Vol. 24, No. 7A, Dec 1981, pp. 3311-3314, 4193.												
RL	C8	Bleiker et al., "A Four State EEPROM using Floating-Gate Memory Cells", IEEE, Vol. SC-22, No. 3, Journal of Solid-State Circuits, June 1987, pp. 460-463.												
RL	C9	Yasuo Tarui, "Japanese Develop Nondestructive Analog Semiconductor Memory", Electronics Review, pp. 29-30, July 11, 1974.												

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Sheet 3 of 6

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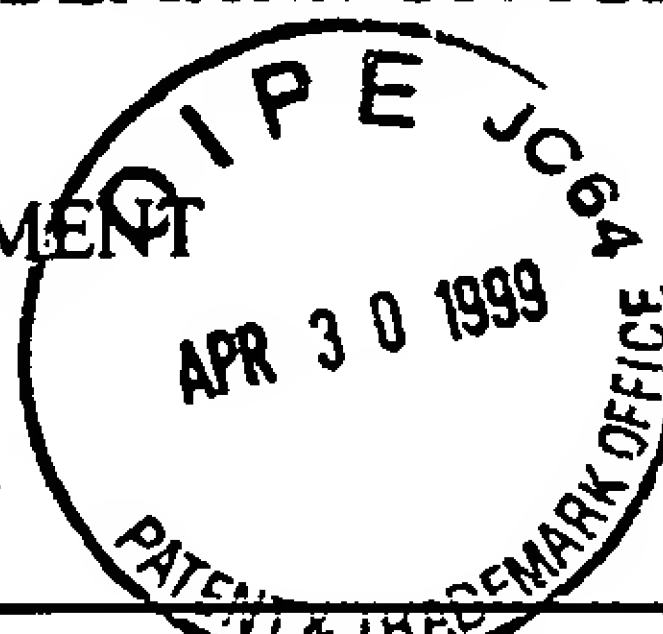
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RV 2/2/11 LWH	A28 4 6 5 2 8 9 7	03/1987	Okuyama et al.			
LWH	A29 4 6 6 3 7 7 0	05/1987	Murray et al.			
LWH	A30 4 6 6 7 2 1 7	05/1987	Janning			
LWH	A31 4 6 8 2 2 8 7	07/1987	Mizuno et al.			
LWH	A32 4 7 1 8 0 4 1	07/1988	Baglee et al.			
LWH	A33 4 7 3 3 3 9 4	03/1988	Giebel			
LWH	A34 4 7 5 7 4 7 4	07/1988	Fukushi et al.			
LWH	A35 4 7 6 3 3 0 5	08/1988	Kuo			
LWH	A36 4 7 7 4 7 0 0	09/1988	Satoh et al.			
LWH	A37 4 8 0 0 5 2 0	01/1989	Iijima			
LWH	A38 4 8 0 3 7 0 7	02/1989	Cordan Jr.			

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS. (YES/N)
LWH B11 JP 58 0 8 6 7 7 7	05/1983	Japan			Abstrac
LWH B12 JP 62 2 8 3 4 9 7	12/1987	Japan			Abstrac
LWH B13 FR 2 4 3 0 0 6 5	01/1980	France			Abstrac
LWH B14 DE 3 2 0 0 8 7 2	07/1983	Germany			Abstrac
LWH B15 EP 0 2 5 1 8 8 9	01/1988	EPO			Abstrac

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

LWH C7	Alberts et al., "Multi-Bit Storage Fet Earom Cell", IBM Technical Disclosure Bulletin," Vol. 24, No. 7A, Dec 1981, pp. 3311-3314, 4193.
LWH C8	Bleiker et al., "A Four State EEPROM using Floating-Gate Memory Cells", IEEE, Vol. SC-22, No. 3, Journal of Solid-State Circuits, June 1987, pp. 460-463.
LWH C9	Yasuo Tarui, "Japanese Develop Nondestructive Analog Semiconductor Memory", Electronics Review, pp. 29-30, July 11, 1974.

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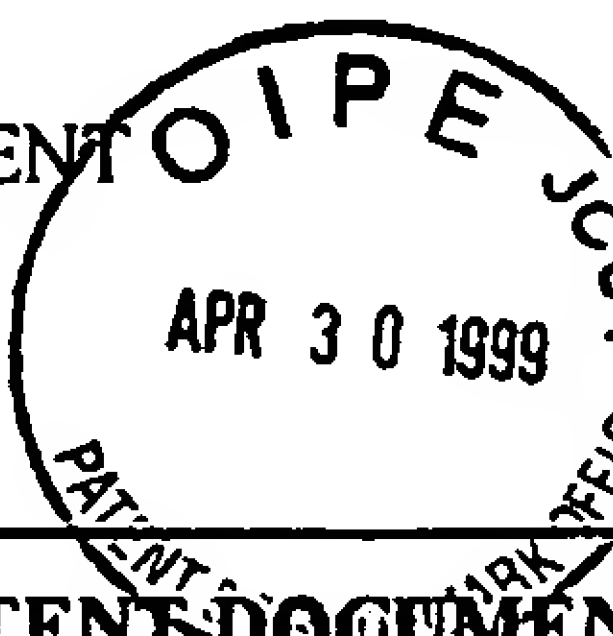
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U. S. PATENT DOCUMENTS							
*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE	
RL 2/2/11 LWH	A39 4 8 6 0 2 2 8	08/1989	Carroll				
LWH	A40 4 8 8 7 2 3 4	12/1989	Iijima				
LWH	A41 4 8 8 8 6 8 6	12/1989	Sinz et al.				
LWH	A42 4 8 9 6 2 6 2	01/1990	Wayama et al.				
LWH	A43 4 9 4 2 5 5 6	07/1990	Sasaki et al.				
LWH	A44 4 9 4 9 2 4 0	08/1990	Iijima				
LWH	A45 4 9 9 2 9 8 4	02/1991	Busch et al.				
LWH	A46 5 0 1 6 2 1 5	05/1991	Tigelaar				
LWH	A47 5 0 4 3 9 4 0	08/1991	Harari				
LWH	A48 5 0 5 1 9 9 4	09/1991	Bluehman et al.				
LWH	A49 5 0 5 3 9 9 0	10/1991	Kreifels et al.				
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LWH	B16 GB 2 2 1 5 1 5 5	09/1989	United Kingdom				
LWH	B17 EP 0 3 4 9 7 7 5	1989	EPO 01/1990				
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)							
LWH	C10	Furuyama et al, "An Experimental 2-BIT/CELL Storage Dram for Macro Cell or Memory-on-Logic Application", IEEE Custom Integrated Circuits Conference, May 1988, pp. 4.4.1 - 4.4.4					
	C11	Horiguchi et al, "An Experimental Large-Capacity Semiconductor File Memory Using 16-LEVELS/CELL Storage", IEEE Journal of Solid-State Circuits, Vol. 23, Feb 1988, No. 1, pp. 27-33.					
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U. S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
RV	A50 5 0 7 0 5 0 2	12/1991	Supnik			
RV	A51 5 1 2 6 9 7 3	06/1992	Gallia et al.			
RV	A52 5 1 3 4 5 8 4	07/1992	Boler et al.			
RV	A53 5 2 1 4 6 5 7	05/1993	Farnworth et al.			
RV	A54 5 2 2 2 1 0 9	06/1993	Pricer			
RV	A55 5 2 4 3 5 7 0	09/1993	Saruwatari			
RV	A56 5 2 6 8 8 7 0	12/1993	Harari			
RV	A57 5 2 7 0 9 7 9	12/1993	Harari et al.			
RV	A58 5 2 7 8 7 9 3	01/1994	Yeh			
RV	A59 5 2 9 3 5 6 0	03/1994	Harari			
RV	A60 5 3 6 9 6 1 5	11/1994	Harari et al.			

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*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
RL	A61 5 3 7 7 1 4 8	12/1994	Rajsuman			
RL	A62 5 3 9 6 4 6 8	03/1995	Harari et al.			
RL	A63 5 4 0 2 3 7 6	03/1995	Horiguchi et al.			
RL	A64 5 4 1 4 6 6 4	05/1995	Lin et al.			
RL	A65 5 4 6 5 2 3 4	11/1995	Hannai			
RL	A66 5 4 7 1 4 3 1	11/1995	McClure			
RL	A67 5 5 3 5 3 2 8	07/1996	Harari et al.			
RL	A68 5 5 6 3 8 3 2	10/1996	Kagami			
RL	A69 5 5 6 8 4 3 9	10/1996	Harari			

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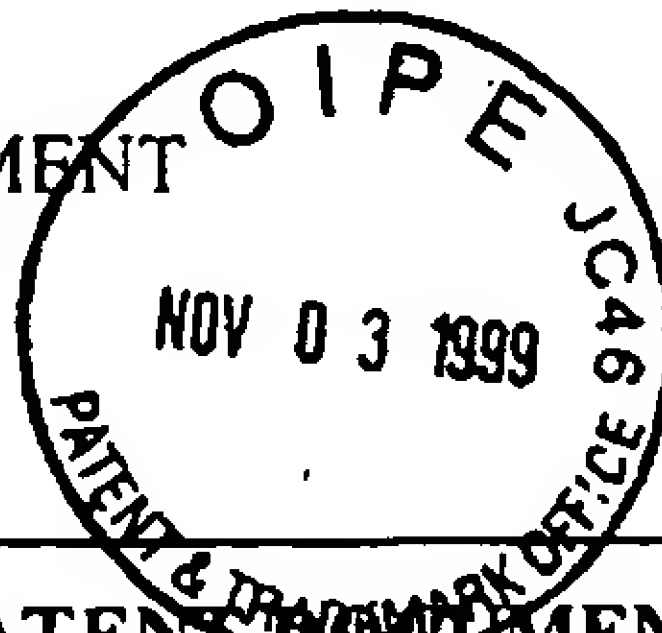
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		FILED September 30, 1999	GROUP 2785



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2/3/11

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
LWH	A70 4 9 3 1 9 9 7	06/1990	Mitsuishi et al.			
LWH	A71 5 2 1 0 7 1 6	05/1993	Takada			
LWH	A72 5 2 9 7 1 0 3	03/1994	Higuchi			
LWH	A73 5 5 4 6 4 0 2	08/1996	Nijima et al.			
LWH	A74 5 5 9 4 6 8 9	01/1997	Kato			

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DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANS. (YES/N)
B18 JP 5 1 8 9 9 8 1	07/1993	Japan			Abstract
B19 JP 58 2 1 5 7 9 4	12/1983	Japan			Yes
B20 JP 58 2 1 5 7 9 5	12/1983	Japan			Yes
B21 JP 59 1 6 2 6 9 5	1983	Japan 09/1984			Yes
B22 JP 59 0 4 5 6 9 5	1982	Japan 03/1984			Yes

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C12	"Gist of Technology in Coding Error Correction", Nippon Kogyo Gijutsu Center Co., Ltd., pp. 109-142.

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